with the command to access the memory array. The memory array is adapted to provide or receive data in response to the command based on at least one of the burst length information and the latency information.

In another aspect of the present invention, an apparatus is provided for accessing a dynamic memory device. The apparatus comprises a memory that is adapted to receive a command from a memory controller to access contents of the memory, receive, from the memory controller, at least one of burst length information and latency information in association with the command to access the contents, and provide data from the memory in response to the command based on at least one of the burst length information and the latency information.

BRIEF DESCRIPTION OF THE DRAWINGS

The invention may be understood by reference to the following description taken in conjunction with the accompanying drawings, in which like reference numerals identify like elements, and in which:

Figure 1 illustrates a block diagram of a system including a device that is capable of accessing a memory, in accordance with one illustrative embodiment of the present invention;

Figures 2, 2A & 2B illustrate ~~Figure 2 illustrates~~ a block diagram of a memory array module of the memory of Figure 1 for supporting memory access at various burst lengths, in accordance with one embodiment of the present invention;

Figure 3 illustrates an exemplary timing diagram of accessing the memory array module of Figure 2 with various burst lengths, in accordance with one embodiment of the present invention;

Figures 4, 4A+4B illustrate

~~Figure 4 illustrates~~ a block diagram of a memory array module of the memory of Figure 1 for supporting memory access with various CAS latency levels, in accordance with one embodiment of the present invention;

Figure 5 illustrates an exemplary timing diagram of accessing the memory array module of Figure 4 with various CAS latency levels, in accordance with one embodiment of the present invention;

Figures 6, 6A+6B illustrate

~~Figure 6 illustrates~~ a block diagram of a memory array module of the memory of Figure 1 for supporting memory access with various write latency levels, in accordance with one embodiment of the present invention; and

Figure 7 illustrates an exemplary timing diagram of accessing the memory array module of Figure 6 with various write latency levels, in accordance with one embodiment of the present invention.

While the invention is susceptible to various modifications and alternative forms, specific embodiments thereof have been shown by way of example in the drawings and are herein described in detail. It should be understood, however, that the description herein of specific embodiments is not intended to limit the invention to the particular forms disclosed,